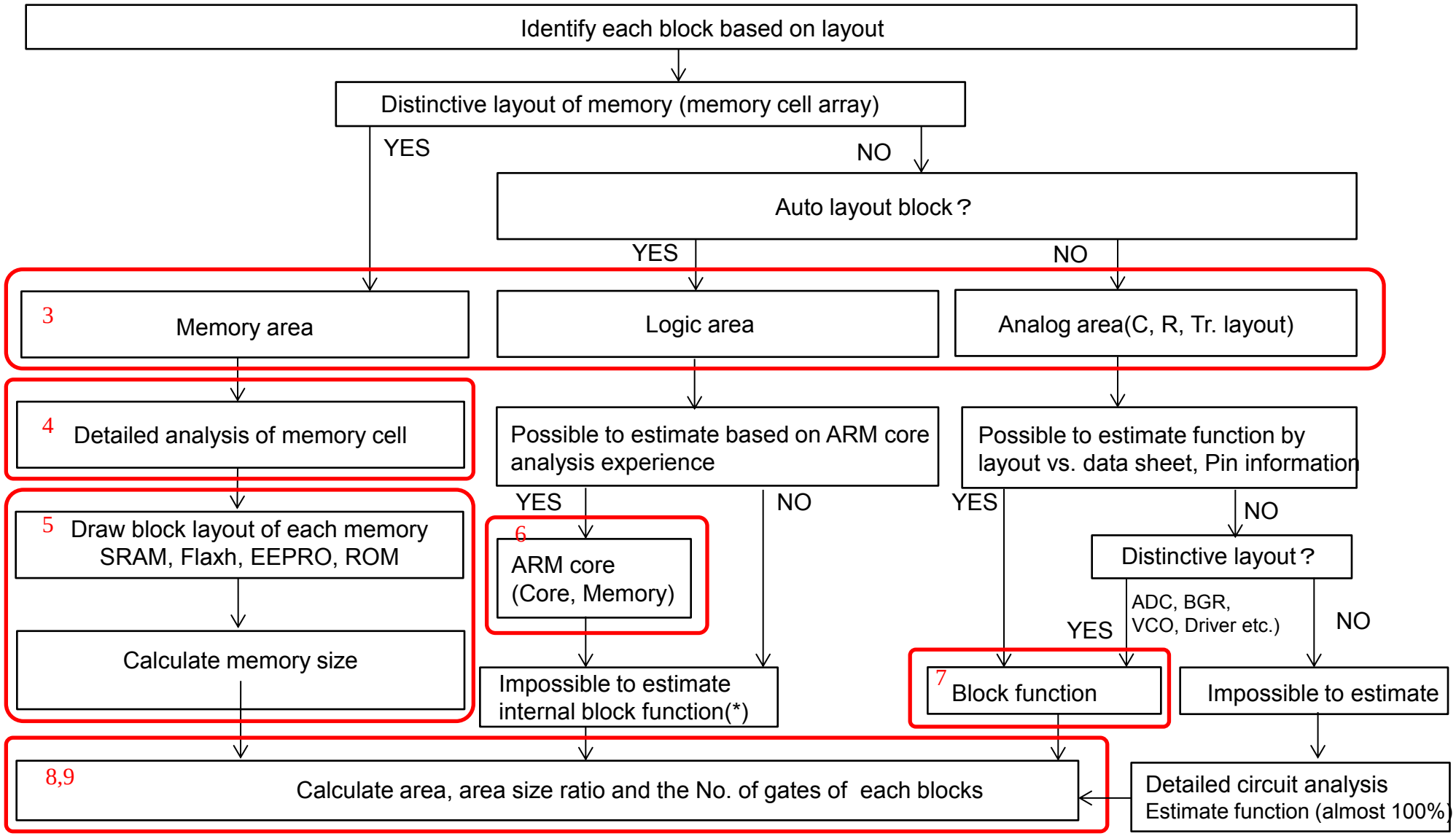
Processor Memory Function Analysis Sample Report

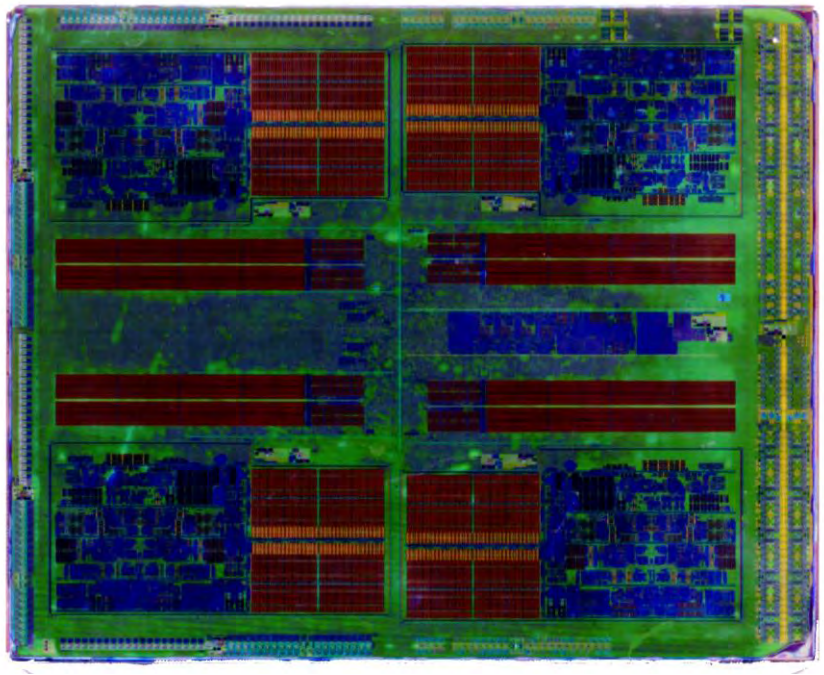
1. Analysis flow chart
2. Analysis example result of XXXXX processor
3. Create block layout of each areas (Analog, IO, Logic, Memory)
4. Detailed analysis of Memory Section
5. Estimation of Memory
6. Layout of core area
7. Estimation of function
8. Calculate each block area
9. Estimate the No. of logic gates

1. Function analysis flow chart

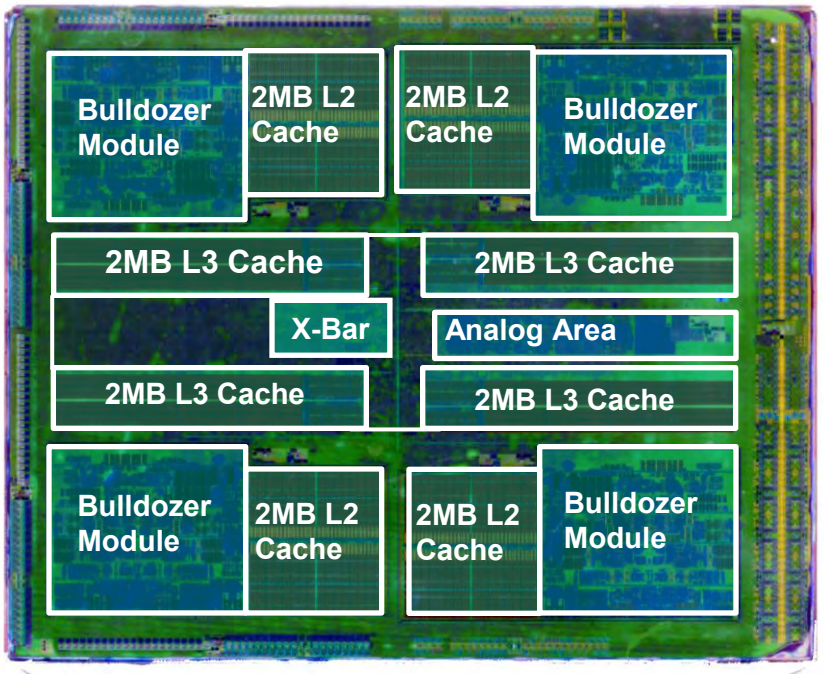


(*)The block function might be fully understood only after detailed circuit analysis is performed

2. Function Analysis Example of XXXXX Processor (not ARM core)



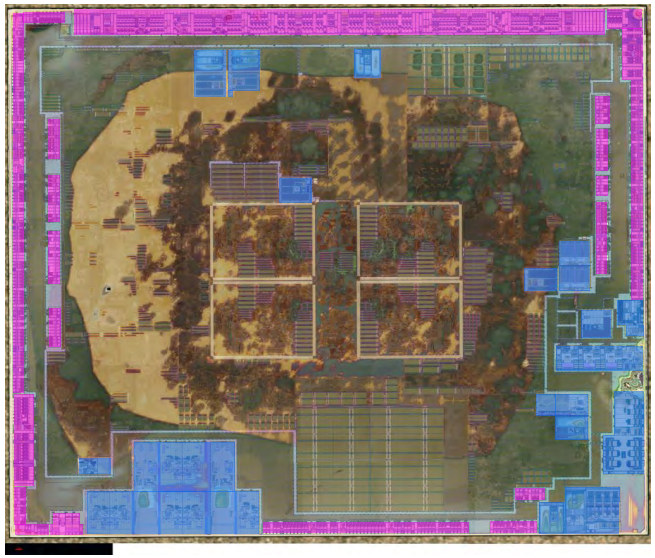
First Metal Layer



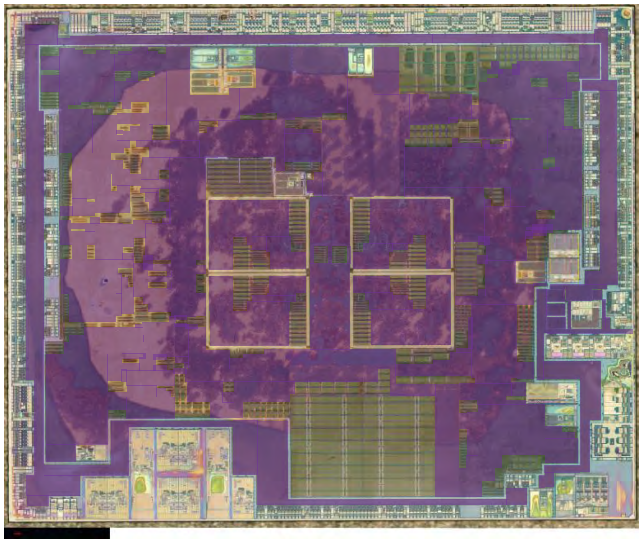
3. Create block layout of each area (Analog, IO, Logic, Memory)

Draw the layout of Analog, IO, Logic, Memory by analyzing gate layer
Memory type is shown by detailed analysis

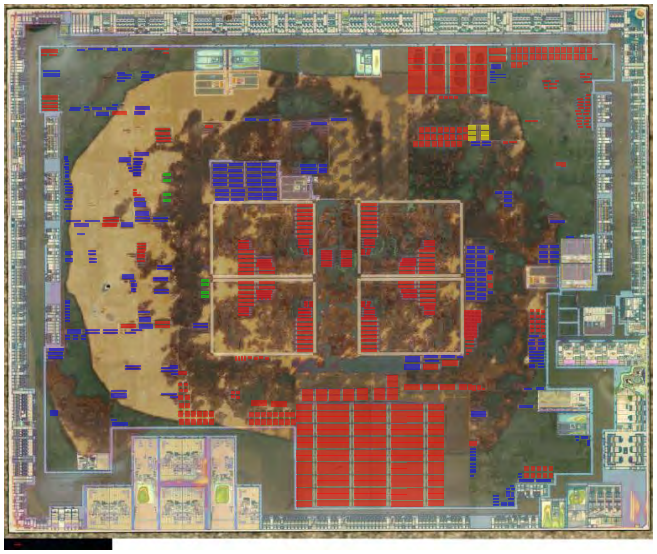
XXXXXX
ARM CORE
Application processor



Analog
IO



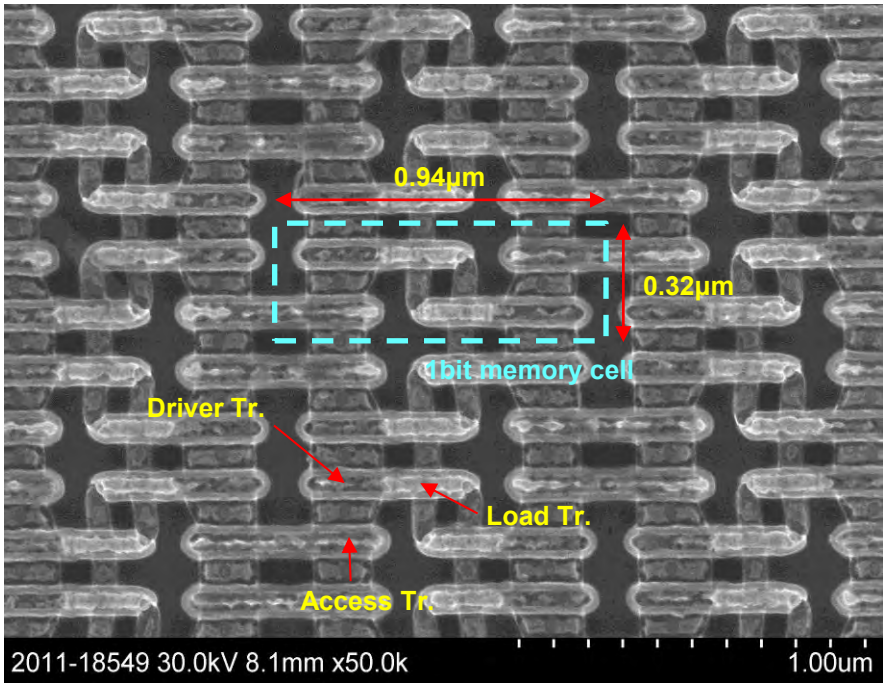
Logic
(=Auto layout area)



6Tr.SP-SRAM
10Tr.SP-SRAM
8Tr.DP-SRAM
ROM

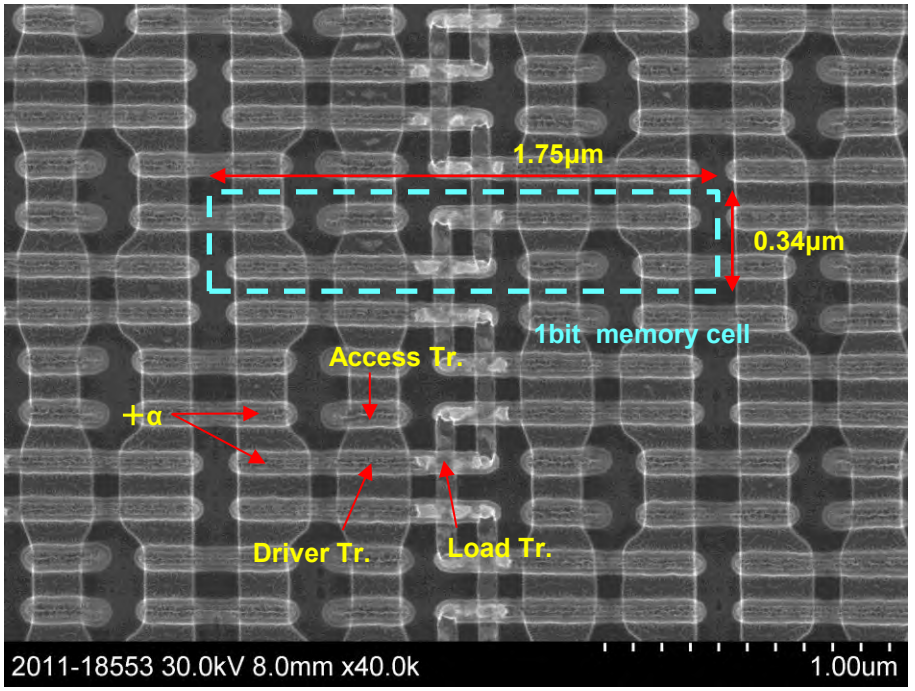
4. Detailed analysis of memory type

1bit size=0.30μm²



6Tr.SP-SRAM

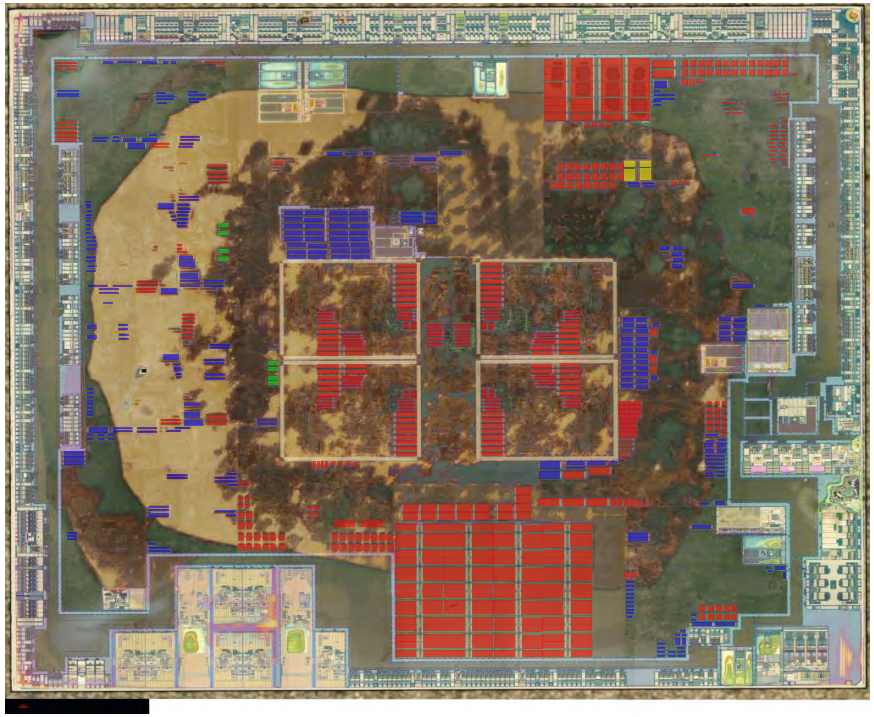
1bit size=0.60μm²



10Tr.SP-SRAM

5. Estimation of memory size

Estimate memory size by using 1bit memory cell size and memory array size



6Tr.SP-SRAM(area1)

10Tr.SP-SRAM(area2)

8Tr.DP-SRAM(area3)

ROM(area4)

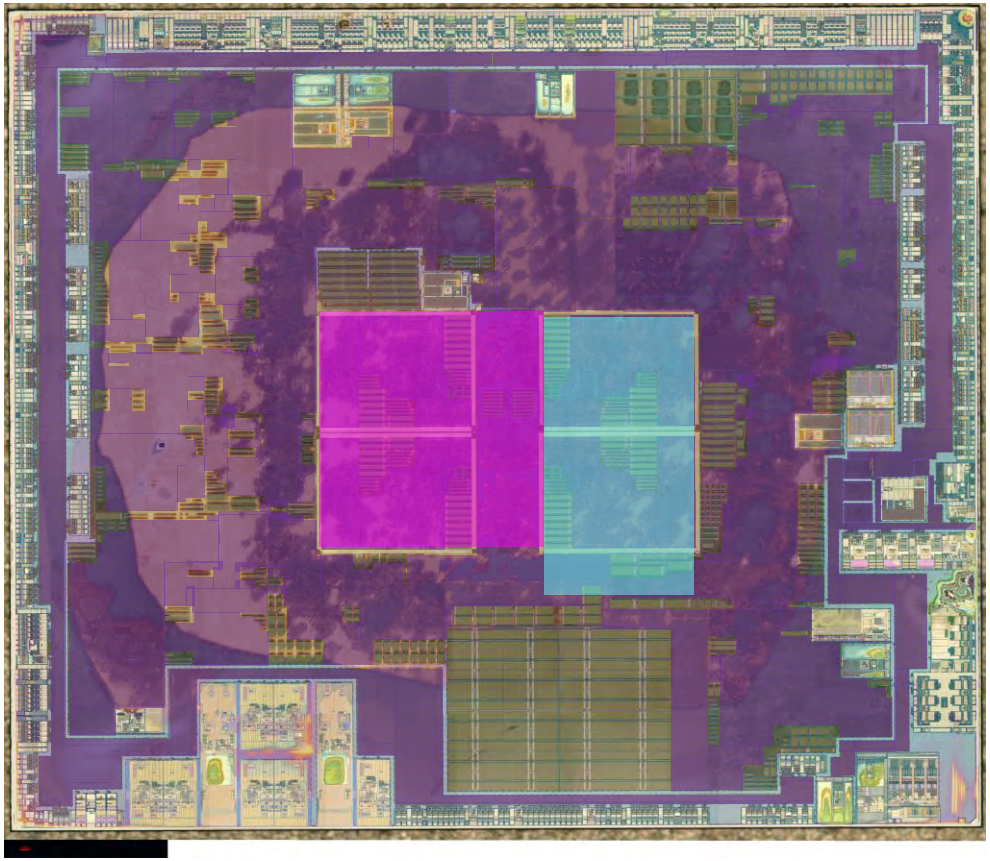
Estimation results

area	size(μm²)	1bit(μm²)	Memory size(bit)
area1	4225912	0.30	17086373
area2	1560716	0.60	1884527
area3	59419	0.60	49032
area4	33578	0.11	487073
		total	19507005

6. Layout of core area

Estimate core area by using data sheet or other information and layout configuration

It is difficult to distinguish form CPU, GPU and DSP without data sheet or other information.



Logic area

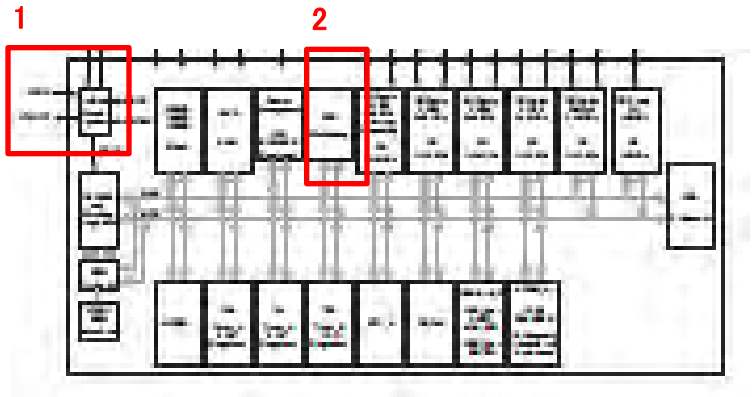
Core region

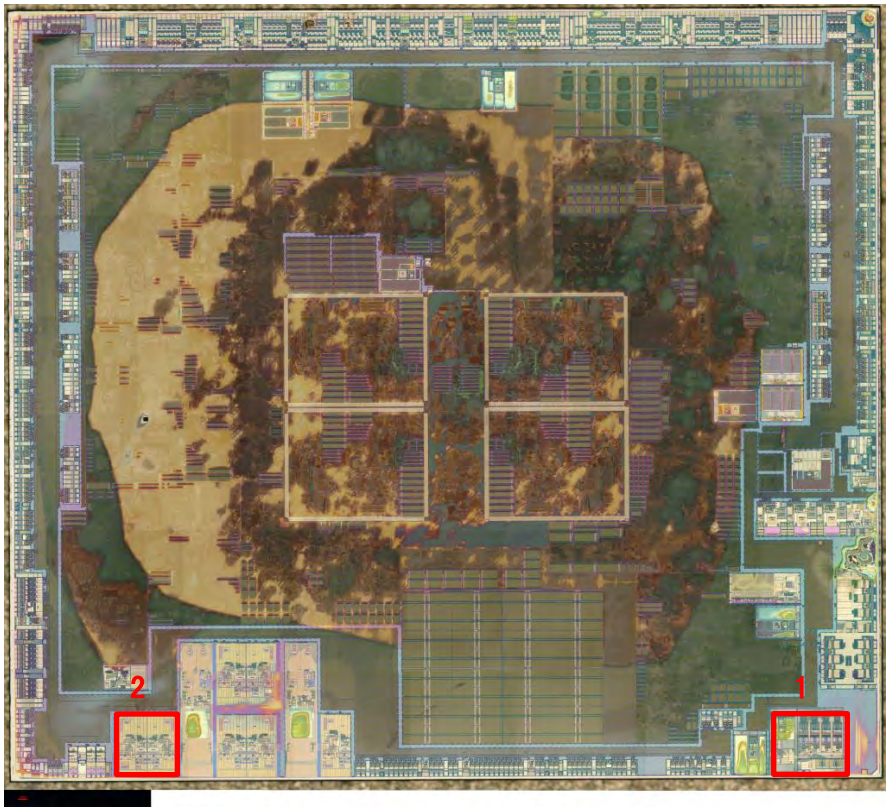
※Note: The above example is just an illustration, not the result of an actual analysis

7. Estimate circuit function

Analog area: To estimate internal block function based on data sheet (block diagram) and layout

Almost impossible to estimate internal block function in the logic area



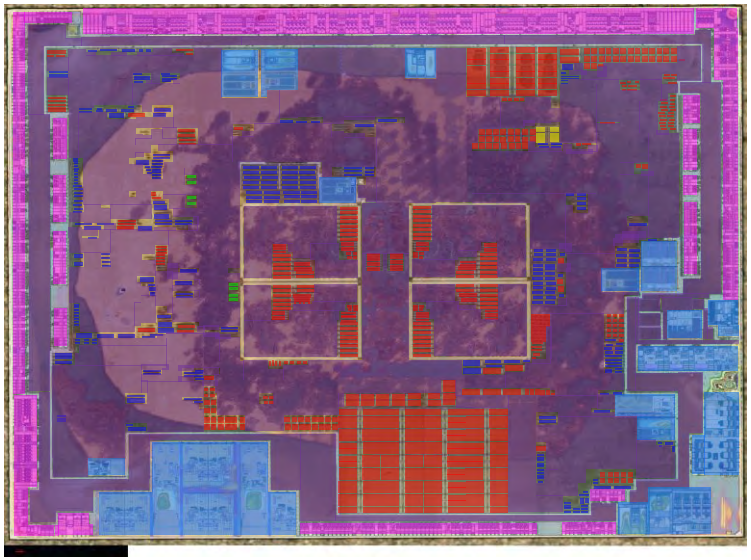


- It is possible to estimate analog block functions having distinctive layout such as BGR, ADC, Driver etc.
- It is possible to estimate analog block function that connect to external pin. (option)

※Note: The above example is just an illustration, not the result of an actual analysis

8. Calculate each block area

※Note: This example is just an illustration, not the result of an actual analysis



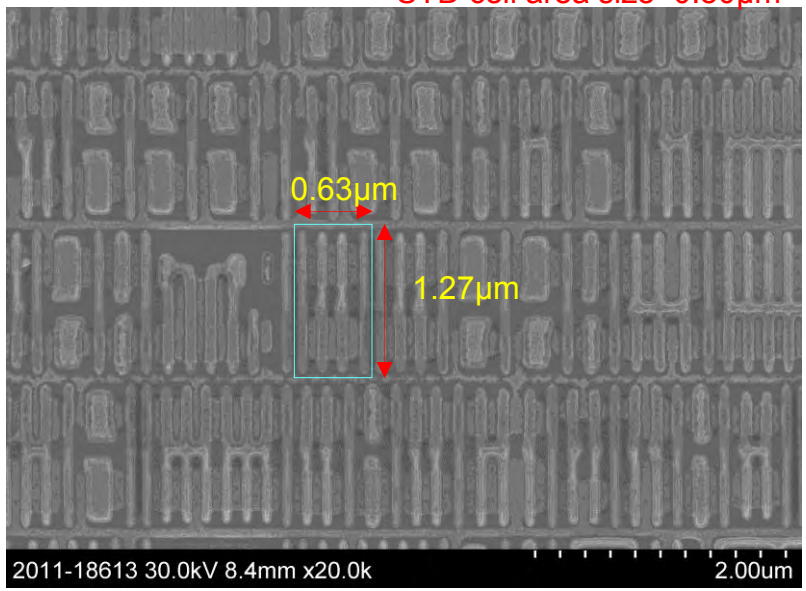
- 6Tr.SP-SRAM(area1)
- 10Tr.SP-SRAM(area2)
- 8Tr.DP-SRAM(area3)
- ROM(area4)
- Logic(area5)
- Analog(area6)
- IO(area7)

	Area size (μm²)	ratio(%)
area1	5625912	6.2
area2	1134716	1.3
area3	48732	0.05
area4	5984	0.06
area5	89285297	70.5
area6	768463	9.2
area7	86458	10.4
Die size	64587	

9. Estimate the number of logic gates

Estimate No. of logic gate of total block by measuring standard cell area

STD cell area size=0.80μm^2



Measure standard cell area size

Calculate the No. of logic gate

Density	area(μm^2)	No. of gates
100%	48284297	72556621
80%	46654237	58795296
60%	38971758	21713972
40%	19314118	36948309
20%	11689059	16571323