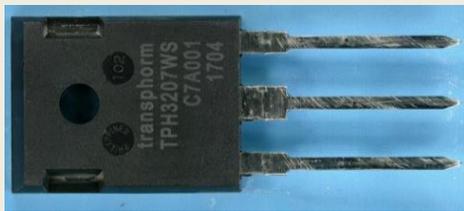
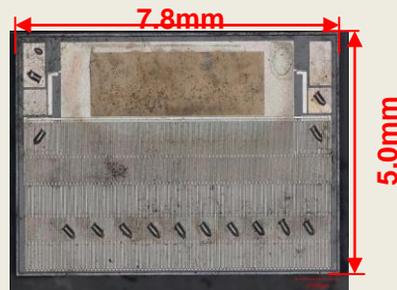


ANALYSIS REPORT OF TRANSFORM 'TPH3207WS' 650V POWER GaN FET

April 2018. LTEC Corporation released a detailed structure analysis report of this 650V GaN FET. This product has 50A output current capability, which is the almost double comparing with other GaN devices. This FET is a cascode arrangement using a low-voltage Si-FET device in order to realize a normally OFF configuration.



Package top view



Die top view

Device features

- Max. operating voltage: 650V, rated DC Drain current $I_D=50A$ at $T_j=25^\circ C$
- ON-resistance, $R_{ON} = 41m\Omega$

Key analysis results

- Actual break-down voltage $BV_{dss}=1700V$. It has wide margin compared with operating voltage specification ($V_{dss}=650$) → Twice larger than other GaN's.
- Countermeasures of device structure and layout for JEDEC compliant
- Stacked structure (GaN device and low voltage Si-FET) to fit in TO-247
- The countermeasure for Gate abnormal oscillation and ringing

The 155 pages report includes

1. The comparison with other GaN power devices,
2. Package cross section and EDX analysis
3. Die plan analysis
4. Die cross section (SEM, TEM), epi layer TEM-EDX material analysis
5. Electrical characteristic measurement (R_{on} , leakage current-vs-temperature, break down voltage and Drain capacitance(C_{oss} vs V_{ds}))

Note: The listed report price may not be accurate as it decreases over time.

Please contact us for current report pricing : info@ltecusa.com

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Note1: Device temperature is as the parameter.

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